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2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/678,523	HOROVITZ, SOREL	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69,71-73,78-81 and 83-96* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7, 11-14, 19-20, 22-25, 29-37, 39-42 and 46-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 1-6,8-10,15-18,21,26-28,38,43-45,54-69,71-73,78-81 and 83-96.

DETAILED ACTION

1. This communication is responsive to Amendment filed 10/14/2008.

2. Claims 1-69, 71-73, 78-81 and 83-96 are pending in this application. Claims 7, 20 and 37 are independent claims. In Amendment, claims 70, 74-77 and 82 are cancelled and claims 1-6, 8-10, 15-18, 21, 26-28, 38, 43-45, 54-69, 71-73, 78-81 and 83-96 are withdrawn from consideration due to previous Restriction/Election. This Office Action is made final.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 7, 11-14, 19-20, 22-25, 29-37, 39-42 and 46-53 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 7, the limitation "empty bit in a register" is not clearly defined in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In addition, the applicant fails to provide a clear definition of empty bit (e.g. as value 0/1 or no value)

within the register nor the support for the clear definition in the original specification for examination purposes. Claims 20 and 37 have the same rejection.

Thus, claims 11-14, 19, 22-25, 29-36, 39-42 and 46-53 are also rejected for being dependent on the rejected base claims 7, 20, and 37.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 11-14, 19-20, 22-25, 29-37, 39-42 and 46-53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 7, the limitation "empty bit" is unclear since it does not clearly define what is the empty bit as whether the empty bit is false bit as 0 or the empty bit is true bit as 1 or the empty bit has no value. For examination purposes, the examiner considers the empty bit in the claim means false bit as 0. In addition, it is unclear how to select the available part know which part has the empty bit in order to select the part. Thus, the claim is also rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the step to determining which part of the parts of the available parts that has the empty bit. Claims 20 and 37 have similar rejection as cited in claim 7. Further, most of the claims do not have structural between features/limitations within the claims.

Thus, claims 11-14, 19, 22-25, 29-36, 39-42 and 46-53 are also rejected for being dependent on the rejected base claims 7, 20, and 37.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 7, 11, 13, 20, 22-24, 29-31, 33, 36-37, 39-41, 46-48, 50 and 53 are rejected under 35 U.S.C. 102(a) as being anticipated by Ott (U.S. 6,477,552).

Re claim 7, Ott discloses in Figures 1-4 a method for finding a next empty bit in a register having N bits and a current pointer pointing to one of the bits (e.g. abstract wherein the empty bit is the zero bit within the nibble and N is equated to 32 bits in the source register rs1 as seen in Figures 1-2), the method comprising:

breaking the N bits of a check vector in the register into M parts, wherein N and M are integers and $1<M<N$ (e.g. Figure 2 wherein 32-bits of source register rs1 are break down into 8 parts and each part consists of 4 bits as nibble to corresponding nibble logics 22x); and

selecting an available part that has a empty bit (e.g. output of the priority encoder in Figure 2 for selecting the part of 0 bit and col. 3 lines 1-25).

Re claim 11, Ott further discloses in Figures 1-4 the available part is a first part, having a empty bit, to the left of the part pointed to by the current pointer (e.g. Figure 4 table).

Re claim 13, Ott further discloses in Figures 1-4 finding a empty bit in the available part (e.g. abstract).

Re claim 20, it is an apparatus claim of claim 7. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 22, it is an apparatus claim of claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 23, Ott further discloses in Figures 1-4 a check sector generator for generating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts (e.g. Figure 2).

Re claim 24, Ott further discloses in Figures 1-4 a second breaker for breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein 0 <=U<=e^y-1, and 0<=L<=2^(x-y)-l, where all of X, Y, U, and L are integers (e.g. Figures 1-2).

Re claim 29, it has similar limitations cited in claim 13. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 30, it has similar limitations cited in claim 11. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 31, it has similar limitations cited in claim 24. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 33, Ott further discloses in Figures 1-4 the empty bit finder finds a empty bit from the beginning of the available part (e.g. Figure 4 table).

Re claim 36, Ott further discloses in Figures 1-4 a next vector generator for generating the next vector with the found empty bit masked (e.g. output of Figure 2).

Re claim 37, it is a means apparatus claim of claim 20. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

Re claim 39, it is a means apparatus claim of claim 22. Thus, claim 39 is also rejected under the same rationale as cited in the rejection of rejected claim 22.

Re claim 40, it is a means apparatus claim of claim 23. Thus, claim 40 is also rejected under the same rationale as cited in the rejection of rejected claim 23.

Re claim 41, it is a means apparatus claim of claim 24. Thus, claim 41 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 46, it is a means apparatus claim of claim 29. Thus, claim 46 is also rejected under the same rationale as cited in the rejection of rejected claim 29.

Re claim 47, it is a means apparatus claim of claim 30. Thus, claim 47 is also rejected under the same rationale as cited in the rejection of rejected claim 30.

Re claim 48, it is a means apparatus claim of claim 31. Thus, claim 48 is also rejected under the same rationale as cited in the rejection of rejected claim 31.

Re claim 50, it is a means apparatus claim of claim 33. Thus, claim 50 is also rejected under the same rationale as cited in the rejection of rejected claim 33.

Re claim 53, it is a means apparatus claim of claim 36. Thus, claim 53 is also rejected under the same rationale as cited in the rejection of rejected claim 36.

Response to Arguments

9. Applicant's arguments filed 10/14/2008 have been fully considered but they are not persuasive.

a. The applicant argues in page 18 last paragraph to first paragraph page 19 for claims rejected under 112 1st paragraph that the empty bit is replaced for the free bit as ordinary skilled artisan would understand the invention which is to find the empty location in a register into which to place a bit. Thus, it should cure the deficiency under 112 1st paragraph as rejected in the last Office action.

The examiner respectfully submits that the applicant points to paragraphs 3, 55 and 57 which do not fully describe the above argument by the applicant. From the above paragraphs [3, 55 and 57], the free bit is a value (e.g. any designated value) from the line indication 608 which points to the free or non-written allocation in the SRAM 605. Thus, the empty bit is nothing to do with the empty location in the register of the bit as argued by the applicant. In addition, the term "empty bit" is just merely disclosed in the background of the invention and does not fully disclosed in the specification which corresponding to the claimed language.

b. The applicant argues in page 21 for claims rejected under 102(a) that the Ott does not disclose or suggest in any way that those arithmetic operations either are for the purpose of or necessarily inherently result in finding of a next empty bit in a register as disclosed in the claimed invention.

The examiner respectfully submits that the applicant does not fully disclose what is exactly the empty bit as the value of the empty bit but rather just points to the paragraphs 3, 55 and 57 and merely states that the empty bit is known to the ordinary skill in the art. The examiner respectfully believes the rejection under Ott is reasonable maintained along with the examiner's interpretation of the empty bit in 112 2nd rejection. In addition, the pointed paragraphs [3, 55 and 57] merely states the empty bit is a bit of the register line indication 608 which is used to corresponding to the non-written buffer of SRAM 605 without further detail the value of that bit. Thus, Ott reasonably discloses a similar method of finding a value, which is a zero value, within a register (e.g. as register line indication 608). Even thought, Ott does not label the bit having the leading zero value as the empty bit, but it has the same meaning which is the zero value.

c. The applicant argues in page 21 last paragraph for claims that the Examiner fails to cite any particular portion of Ott '552 for finding the next empty bit in a register and breaking a check sector into parts does not identify an empty bit in a register. Further, the Examiner does not appear to have cited Ott '828.

The examiner respectfully submits that the Examiner has an option to use new reference Ott '552 in the non-final Office action. Further, the independent claims 7, 20 and 37 do not define the detail structure of how finding a certain bit in a register, but rather just break down into several parts and select a part as the certain which clearly seen in the Ott's reference which break the vector into multiple nibble of 4-bits and selecting a nibble having the leading zero value as the empty bit in the vector as the register.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

December 18, 2008